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09/853,005	05/09/2001	Chau-Chad Tsai	JCLA5312	5161

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EXAMINER	
BAKER, PAUL A	

ART UNIT	PAPER NUMBER
2188	13

DATE MAILED: 03/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/853,005	TSAI ET AL.	
	Examiner	Art Unit	
	Paul A Baker	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-16* is/are allowed.

6)☒ Claim(s) *1-10,12-13* is/are rejected.

7)☒ Claim(s) *11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted (Taiwan 89111825) under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Acknowledgment is made of applicant's claim for priority under 35 U.S.C. 119(a)-(d) based upon an application 87119245 filed in Taiwan on 20 November 1998. A claim for priority under 35 U.S.C. 119(a)-(d) cannot be based on said application, since the United States application was filed more than twelve months thereafter.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 – 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ziegler et al. US Patent 6,182,176.

In regards to claim 1, Zeigler discloses a cache system inside the peripheral device interface control chip (figure 2 element 116) of a computer system that includes a memory unit (figure 2 element 115), a central processing unit (CPU) (figure 2 element 120), a CPU bus (figure 2 element 112), a peripheral bus device (figure 2 element 160), comprising:

A data buffer located within the control chip for holding a data stream read from the memory unit so that data required by the peripheral device bus are provided (figure 2 element 166), and when the data stream is synchronous (applicant interprets "synchronous" to mean "coherent with memory" this fits more closely with the applicant's disclosure) with data in a corresponding address within the memory unit (column 4 lines 30 – 42), the data stream is retained, and when any one of the peripheral devices demands data already in the data stream, data within the data stream can be immediately provided by the data buffer so a latency period for retrieving the data stream from memory again is reduced is inherent since a data stream present on the queue (figure 2 element 166) will be ready for transmission when requested by I/O bus (figure 2 element 166); and

a peripheral device interface controller for determining if the data stream includes data demanded by a particular peripheral device and determining if the data stream is synchronous with data in the corresponding address, then retrieving the data stream from the memory unit and putting the data in a data buffer, and finally switching a state of that portion of the data buffer having data stream therein (figure 2 controller sub-element within element 114).

Zeigler does not disclose the peripheral device interface controller installed within the control chip. However it is well known in the art the benefit for incorporation of separate modules that are in direct communication on the same chip. These benefits include a faster rate of communication between the modules because reduced stray capacitances on the communication lines results in higher slew rates, and reduced

production costs from only having to bond and package one integrated circuit instead of two.

In regards to claim 2, Zeigler discloses the peripheral device interface controller further includes transmitting a probe-hit-read signal to the central processing unit in column 9 lines 21 – 23.

In regards to claim 3, Zeigler does not disclose the peripheral device interface controller further includes receiving signals emitted when data are written from the peripheral device bus to the corresponding address. However it is well known in the art the necessity indicating the completion of an I/O operation, the two primary means of doing so are the assertion of an signal and the alteration of a special status register, the former is used when the information must be transmitted between modules and the latter is typically used in intra-module communication and also involves a signal asserted but that signal is stored so that a processor may check the status at a latter point in time. Both means of communicating the writing of data from the peripheral device bus to a corresponding address involve the assertion of a signal. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a signal emitted when data is written from the peripheral device bus to the corresponding address for the purpose of notifying the action's completion.

In regards to claim 4, Zeigler discloses the peripheral device interface controller further includes receiving signals emitted when data are written from the CPU bus to the corresponding address in column 6 line 66 through column 7 line 20.

In regards to claim 5, Zeigler discloses the peripheral device interface controller further includes receiving signals emitted when data are read from the corresponding address to the CPU bus.

In regards to claim 6, Zeigler discloses the data buffer comprises at least one line (figure 2 element 166) caches require the existence of at least one line.

In regards to claim 7, Zeigler does not disclose the data buffer has altogether eight lines. However, the choice of the depth of the data buffer is matter of design, and the exact number is relatively arbitrary (the choice of a larger buffer reduces the likelihood of a cache miss, while the choice of a smaller buffer reduces the physical size and cost of the system). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to set the depth of the data buffer to eight lines for the purpose of limiting the amount of memory required for the implementation of the data buffer.

In regards to claim 8, Zeigler does not disclose the eight lines are divided into four transmission blocks each having two lines. However it is well known the use of

direct mapping caching scheme for placing data objects within a cache. Peripherals on the I/O bus have a unique identifier (address) the use the well known 2-way direct mapped caching scheme (depth of four) would result in four transmission blocks each having two lines. Zeigler does not disclose the exact means of placement of data within a cache block suggesting a plurality of possible schemes. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the eight lines divided into four transmission blocks for the purpose of reducing the complexity of placement logic.

In regards to claim 9, Zeigler does not disclose each line comprises of 32 bytes. However, it is well known in the art that the cache line has a power of two width so that the least significant bits of an address provide an index into the cache line. The currently most popular cache line widths are 32 and 64 bytes. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to comprise each line of 32 bytes.

Claims 10, 12, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ziegler et al. US Patent 6,182,176, in view of Handy "The Cache Memory Book".

In regards to claim 10, Ziegler discloses method of synchronization data transmission between cache memory inside a peripheral device interface control chip (figure 2 element 116) and external device that can be applied to a computer system

having a memory unit (figure 2 element 115), at least one central processing unit (figure 120 element 120), a control chip (figure 2 element 114), a peripheral device bus (figure 2 element 160), a CPU bus and at least one peripheral device (figure 2 element 112), a memory data stream becomes a cache data stream when the memory data stream within the memory is read into the central processing unit, and the memory data stream becomes a buffer data stream when the memory data stream is read into the data buffer (figure 2 element 166).

Zeigler does not disclose the control chip includes a peripheral device interface controller and a data buffer and the central processing unit uses a MOESI protocol, and

when the cache data stream is in a modified state and if the data buffer executes a read operation from an address in memory that corresponds to the cache data stream, the peripheral device interface controller inform the central processing unit to set the cache data stream into an owner state; and

when the cache data stream is in an exclusive state and if the data buffer executes a read operation from the corresponding address, the peripheral device interface controller will inform the central processing unit to set the cache data stream into a shared state.

It is well known in the art the benefit for incorporation of separate modules that are in direct communication on the same chip. These benefits include a faster rate of communication between the modules because reduced stray capacitances on the communication lines results in higher slew rates, and reduced production costs from only having to bond and package one integrated circuit instead of two.

Handy discloses the MOESI protocol on page 165 – 169, while Zeigler states that cache coherency is maintained in column 3 lines 51-55 but he does not directly disclose the exact protocol for maintaining coherency in the cache, MOESI is one of the two most popular protocols implemented in the current state of the art. The disclosure of snooping (column 4 lines 33 – 38) which is necessary for the implementation of the MOESI protocol suggests Zeigler's disclosure is sufficiently enabled to implement the MOESI protocol. Handy also discloses in table 4.3 on page 167 under the **From System Bus** heading "Read Hit" row "Modified" column shows that a read hit on a Modified cache line will update the status to Owned, and "Exclusive" column shows that a read hit on an Exclusive cache line will update the status to Shared. With the MOESI protocol implemented within Zeigler this would lead to informing the central processing unit to set the cache data stream to an owner state when the cache data stream is in a modified state and the data buffer executes a read operation from an address in memory that corresponds to the cache data stream, and informing the central processing unit to set the cache data stream into a shared state when the cache data stream is in an exclusive state and if the data buffer executes a read operation from the corresponding address. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the MOESI protocol for the purpose of maintaining cache coherency.

In regards to claim 12, Zeigler discloses a probe-hit-read signal is transmitted from the peripheral device interface controller to the central processing unit when a

buffer data stream is read from the peripheral device interface controller to the data buffer in column 9 lines 21 – 23.

In regards to claim 13, Zeigler does not explicitly disclose the probe-hit-read signal further includes the corresponding addresses however the CPU needs to know where the data stream is located within the data buffer. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the corresponding address for the purpose of notifying the CPU the location on the data stream.

Allowable Subject Matter

Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 14-16 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

In regards to claim 14, none of the prior art of record discloses the cache coherency state transition matrix specified on page 20 line 1 through page 21 line 3 in combination with applicant's specified structural elements as detailed on page 19 lines 18 - 24. Islam et al. US Patent 6,032,228 provides a method for implementing

applicant's cache coherency state matrix (CCSM) but fails to describe applicant's specific CCSM.

Claims 15 and 16 are allowable as being dependent upon claim 14.

Response to Arguments

Applicant's arguments filed 23 December 2003 have been fully considered but they are not persuasive.

Zeigler states in column 1 lines 47-55 "*In the case of a shared memory multi-processor computer in which each processor has cache memory, the situation is somewhat more complex. In such a computer, the most current data may be stored in one or more cache memories, or in the main memory. Software executing on the processors must utilize the most current values for data associated with particular addresses. Thus, a "cache coherency scheme," must be implemented to assure that all copies of data for a particular address are the same.*" Zeigler ***clearly*** states that data is being stored in the cache memories and when he specifies cache coherency queues he is not referring to queues containing cache coherency information but queues of data which is coherent with other copies of the data within the system.

Because the applicant has found a definition of a cache which contradicts examiners provided definition does not nullify examiner's definition. By applicant's interpretation Zeigler's element 166 cannot be a cache because it is not situated between a processor and a bus. Applicant's provided definition is antiquated and does

not reflect the current state of the art, caches are used in many situations today that do not fit the IEEE definition (ie NAT caches located inside network routers).

Zeigler's choice of placement of the controller is irrelevant to the operation of Zeigler's invention, placing the portion of the controller which is responsible for the operation and coherency of the I/O module (controlled by element 140 of figure 2) into the I/O module would not render Zeigler's invention inoperable.

It is notoriously well known in the art that when Zeigler mentions throughout his specification the use of a cache coherent scheme that ***any*** cache coherency scheme may be used (of which MOESI belongs) it is not necessary for Zeigler to explicitly mention MOESI for one of ordinary skill in the art to understand that MEOSI would be a obvious choice for a cache coherency scheme.

For these reasons the examiner maintains his previously held rejections.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul A Baker whose telephone number is (703)305-3304. The examiner can normally be reached on M-F 10am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703)306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PB

Mano Padmanabhan 3/22/04

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TC 2100